PVA TePla

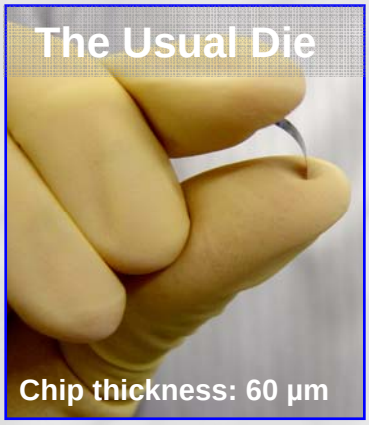
Division Plasma Systems

Advanced Concepts in Remote Cold Dry Etching for

Ultra Thin Wafers and Chips

Main Applications

- Wafer Level Stress Relief
- Chip Level Stress Relief (CSH)
- Post Polish Treatment / Pre-Backmetal
- Wafer Thinning
- Surface Passivation
- Surface Cleaning



Chip with backside stress relief only

Chip with backside stress relief and with CSH

Advantages

- Ideal Dies for 3D Interconnect Stacking
- Processes fit to low cost consumables
- Best CoO available: 40 w/h @ 3 µm etch
- OEM and Stand-alone
- No direct plasma on chip
- No wet chemicals or water

ASYNTIS 2.2
The High Throughput Dry Etcher

ASYNTIS 4008
The Cost Effective Dry Etcher

Wafer Level Stress Relief

applicable to ground wafers:
- on backgrinding tapes
- on hard support and ring carriers
- as carrier-free wafers

Post Polish Treatment

applicable to thinned wafers:
- as pre-metal step on shiny surfaces

Chip Level Stress Relief (CSH)
(Chip Side Healing)

applicable to singulated substrates (blade/laser):
- as single chips on tape
- as singulated wafers on dicing tape
- as singulated or partially diced wafers on grinding tape

Surface Passivation

applicable to wafers and chips:
- seals against contamination
- generates hydrophilic surface

Substrate Thinning

applicable to:
- down to 10 µm thickness
- to any substrate size up to 12” wafers
- single relocated chips on tape

Surface Cleaning

applicable to wafers and chips:
- eliminates loose organic material
- prepares the substrates for etching

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